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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,995	03/11/2004	Motoki Kanamori	XA-9632A	4642

181 7590 07/01/2005

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,995	KANAMORI ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-19* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/082,310.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Request for Continued Examination, RCE, filed June 10, 2005 has been entered.

2. Claims 1 – 10 have been canceled. New claims 17 – 19 have been added.

3. Claims 11 – 19 are presented for the examination.

Claim Objections

4. Claims 13 and 18 are objected to because of the following informalities:

In claim 13, line 6, it is believed that the 'status **flag**' was meant to mean the 'status indication', whose antecedent basis was introduced in line 3, and also to be consistent with 'status indication' in line 3 of claim 14.

In claim 18, lines 3 – 4, it is also believed that '...a **value**...' was meant to mean '... a signal...', for consistency with line 5.

The remainder of the Action is examined in accordance with the meaning as indicated, unless they are meant otherwise. And appropriate correction is nevertheless, required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 11 – 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kaki et al. (US Pat 6,549,974 B2).

Regarding claim 11, Kaki et al. disclose a non-volatile storage device, comprising:

a controller (fig. 1, processor 2);

a buffer memory (fig. 1, write buffer memory 5);

a nonvolatile memory (fig. 1, flash memory 4);

wherein said buffer memory comprises a plurality of banks (col. 4, lines 39 – 42, the write buffer memory ... a plurality of sectors in units of 512 bytes, which are considered as the plurality of banks. See also col. 5, lines 20 – 31, 3 areas of buffer memory 5 corresponds to the 3 sectors of data); and

wherein said controller performs control operations to receive data from outside of said nonvolatile storage device, to store received data to said banks of said buffer memory, and to write received data from said banks of said buffer memory to said nonvolatile memory (col. 9, lines 57 – 60);

wherein said controller detects whether received data has been written from each bank of said buffer memory to said nonvolatile memory (col. 5, lines 48 – 61), and performs control operations to select one of said banks of said buffer memory that is not storing received data yet (col. 9, lines 52 – 65) for storing further received data to be

written to said nonvolatile memory (col. 6, lines 30 – 49, '... the data of more sectors can be similarly written'. See also col. 9, line 66 – col. 10, line 24, '... the processor 2 then determines if additional data to be written remain.'), and

wherein said controller provides a signal to the outside of said nonvolatile storage device when said controller detects that all of said banks of said buffer memory are storing received data yet to be written to said nonvolatile (col. 5, lines 27 – col. 6, line 7, and also col. 6, lines 30 – 34. One word of 512 bytes fills up one block of the buffer memory 5 before it is written to the flash chips).

Regarding **claim 12**, Kaki et al. also disclose the nonvolatile storage device according to claim 11, wherein a total storage size of all banks of said buffer memory equals a size of a unit of data that is written into said nonvolatile memory at a time (col. 5, lines 13 – 26).

Regarding **claim 13**, Kaki et al. also disclose the nonvolatile storage device according to claim 11, further comprising:

a status register including a status indication which indicates whether a transfer of data from said buffer memory to said nonvolatile memory has been completed, wherein said status indication (incorrectly written as flag) is set by said controller (col. 3, lines 31 – 58, status polling serves for the processor to determine that the operation of writing the data into the flash memory chip has ended. See also col. 9, line 66 – col. 10, line 4).

Regarding **claim 14**, Kaki et al. also disclose the nonvolatile storage device according to claim 13,

wherein the status indication includes a plurality of flags respectively corresponding to said plurality of banks of said buffer memory (col. 9, line 66 – col. 10, line 4. Each flash memory chip #0, #1, and #2 has a status polling—flag), and

wherein each of said flags indicates whether transferring of data from the corresponding bank of said buffer memory to said nonvolatile memory has been completed (col. 10, lines 4 – 24. A minus number registered as the counter value when write operation is not ended yet—not completed, and when the write operation is complete, the counter value is incremented).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaki et al. in view of Tobita et al. (US Pat Pub 2002/0051394 A1).

Regarding **claim 16**, Kiaki et al. disclose the non-volatile storage device according to claim 11, further comprising:

a register in which an address range of said non-volatile memory is set (fig. 1, address controller 31, col. 4, lines 53 – 56).

Although Kaki et al. did not clearly disclose data detection means for detecting whether data may be stored in said non-volatile memory based on the address

information that is set in the register...; however, this feature has been shown by Tobita et al. (paragraph 0329, "... data amount does not exceed a predetermined value", and paragraph 0036).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the feature taught by Tobita et al. to the disclosure by Kaki et al., so that non-volatile storage device would operate more efficiently and prone to less possible errors.

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaki et al. in view of Kibayashi et al. (US Pat Pub 2001/007533 A1).

Regarding **claim 17**, Kaki et al. disclose a nonvolatile memory apparatus, comprising:

a controller (fig. 1, processor 2);

a plurality of memory memory areas (fig. 1 and col. 5, lines 20 – 31, write memory buffer 5 having 3 blocks);

and a nonvolatile memory (flash memory 4),

wherein said controller is capable of receiving an arbitrary one of commands including a write command, and is adapted to perform an operation in response to a received command (col. 9, lines 57 – 65, processor 2 receives write request and performs data transfer processes),

wherein in a write operation in response to receiving said write command, said controller operates to receive data for storing to a first memory area of said plurality of

memory areas (abstract and col. 9, line 57 – col. 10, line 4, one word of 512 bytes per block in the buffer memory 5 is filled up before it can be transferred to the flash memory), to receive data for storing to a second memory area of said plurality of memory areas after receipt of the data for storing to said first memory area, and to transfer data stored in said first memory area in parallel to said nonvolatile memory during receiving of the data for storing to said second memory area if said nonvolatile memory is ready to receive data (abstract and col. 2, lines 44 – 59, write operations carried out in parallel, or overlapped in time, manner).

Although Kaki et al. did not clearly teach wherein the controller is adapted to sat a signal which can be output in response to a request from outside said nonvolatile memory apparatus, when data stored in said plurality of memory areas cannot be transferred to said nonvolatile memory under a condition that said nonvolatile memory is not ready to receive data. However, this feature has been taught by Kobayashi et al. (paragraph 0006, '... controller 1 checks the operation state of flash memory chip n, and it branches to the direction of ... **Busy if the chip has Busy status'**).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature taught by Kobayashi et al. to the invention by Kaki et al., so that increase speed in write operation is accomplished (paragraph 0007).

Also, with respect to the feature in which the controller having a plurality of memory areas, or the memory areas are included in the controller, although Kaki et al. did not clearly indicate that the buffer memory 5 could also be combined with the

processor 2. Nonetheless, it would have been obvious to one having ordinary skill in the art at the time the invention was made, to include the buffer memory 5 together with the controller processor 2, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

10. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaki et al. and Kibayashi et al., and further in view of Ko (US Pat 6,128.675).

Regarding **claim 18**, Kaki et al. and Kibayashi et al. disclose the nonvolatile memory apparatus according to claim 17, except wherein said controller comprises a register of which a signal can be output to the outside thereof, and wherein said signal is a value of said register. However, this feature has been taught by Ko (fig. 2 shows the structure of flash memory control circuit 180 of fig. 1, of which latches 181, 183, and 185 are illustrated. One exemplary latch is latch 183, whose output value is the ALE signal).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature shown by Ko to the processor/controller by Kaki et al. and Kobayashi et al., so that flash memory chips are operate by commands of the controller (Ko, col. 4, lines 2 – 17).

With respect to **claim 19**, Kaki et al. show in col. 9, lines 57 – 65, that the processor 2 receives write request and data transfer from the standard bus 1. It is then considered inherent that nonvolatile memory apparatus according to claim 18 further

comprises a data terminal for receiving data corresponding to said write command, which is received through the command terminal.

Allowable Subject Matter

11. **Claim 15** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

The prior arts teach a nonvolatile storage device/apparatus as entailed above, further comprising:

a first register containing information which indicates whether each of said banks of said buffer memory is storing received data, and

a second register containing information which indicates whether received data stored in each of said banks of said buffer memory has been transferred to said nonvolatile memory,

wherein said controller judges whether each of said banks of said buffer memory stores received data yet to be transferred to said nonvolatile memory, based on information contained in said first register and information contained in said second register, for setting each of said flags of said status indication.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham LP
June 25, 2005

HOAI HO
PRIMARY EXAMINER